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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/057,738	WOLRICH ET AL.	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,13,16-21,26-29,33-35,37,40,41,43-45,49-51 and 53-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,13,16-21,26-29,33-35,37,40-41,43-45,49-51 and 53-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed on 17 March 2008. Claims 1-7, 13, 16-21, 26-29, 33-35, 37, 40-41, 43-45, 49-51 and 53-65 are pending. Claims 8-12, 14-15, 22-25, 30-32, 36, 38-39, 42, 46-48 and 52 are cancelled. All objections and rejections not repeated below are withdrawn.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 26 recites "[a] machine-accessible medium, which when accessed results in a machine performing operations". The specification fails to disclose any medium which can be construed as a machine-accessible medium which when accessed results in a machine performing operations. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 26-29, 45 and 59 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 26 recites "[a] machine-accessible medium, which when accessed results in a machine performing operations". The specification fails to disclose any medium which can be construed as a machine-accessible medium which when accessed results in a machine performing operations.

All dependent claims are rejected as having the same deficiencies as the claims they depend from. Appropriate correction is required.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 28-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 28 and 29 recite the limitation "[t]he computer program product of claim 26" on line 1 of each claim. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. Claims 13, 49, 55, 56 and 61-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Correale, Jr. et al. [US 6,587,905 B1] (hereinafter "Correale").

Per claims 13, 49, 55, 56 and 61, Correale teaches a data processor (see Correale, claim 4, "a data processing system", the processor is considered to be including the CPU, other Master devices, and the PLB Arbiter) comprising:

a plurality of programming engines (see Fig. 10, the Master devices);

a push arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of an unidirectional push bus (see Fig. 10, rdDBus and rdDBusAux) by a plurality of external memory resources that are external to the data processor (see Fig.10, the slave devices) in which requests for using the push bus are sent from the memory resources (when an unbalance in read and write traffic occurs, an Auxiliary_read 104 signal is broadcast to all slave devices, and one of the slave devices claims this read cycle and gain access to the auxiliary read data bus to transmit read data, therefore it should be clear that this teaching indicates there must have been at least one request to claim the cycle and bus from each slave device that is serving a read operation and has data to provide to the bus; the auxiliary read bus can be considered as part of the unidirectional push bus

since it is merged with the rdDBus to feed data into rdDBus0-N ports of the master devices; see col. 4, lines 10-19 and lines 53-67 to col. 5, lines 1-42 and Fig. 10), the push bus arbiter being internal to the data processor (see col. 4, lines 1-6, PLB and its arbiter are comprised within the processor architecture), the push bus to push data from the memory resources to an input transfer memory (not clearly shown by Correale in its drawings, but it is clear that a register must be present on a processor's input port which is connected to a data bus in a processor architecture, because processors can execute instructions and fetch data much faster than memories can be accessed to provide the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a system clock) associated with the programming engines; and

a pull bus arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of a unidirectional pull bus (see Fig. 10, wrDBus) by the external memory resources in which requests for using the pull bus are sent from the memory resources (Correale also teaches the write bus can be used in place of the auxiliary read bus when the write bus is implemented as a tri-state bus, and it is clear that a tri-state bus is always unidirectional when set in a particular state; therefore it is also clear that there must have been at least one request for using the pull bus from the slave devices serving read operations since only one of them can claim the read cycle and the write bus to provide read data; see col. 5, lines 43-53; col. 4, lines 10-19 and lines 53-67 to col. 5, lines 1-42 and Fig. 10), the pull bus arbiter being internal to the data processor, the pull bus to pull data from an output transfer memory (not clearly shown by Correale, but it is clear that a register must be

present on a processor's output port which is connected to a data bus in a processor architecture, because processors can execute instructions and provide read/write data much faster than memories can be accessed to provide or store the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a clock) associated with the programming engines and to transfer the data to the memory resources.

Per claims 62 and 64, Correale further teaches that the memory resources comprise random access memory devices. Correale clearly teaches the slave devices are accessed by the masters for data read and write operations, which indicates the slave devices can be memory/storage devices. Correale further teaches one of the slave devices is a memory controller (see col. 5, lines 55-60) and one of the peripheral devices connected to the masters is RAM 614 (see Fig. 6), and it should be clear that RAM 614 is controlled by a memory controller and the data that are written or read by the master devices are actually stored to or provided from the actual memory device such as RAM 614. Therefore, it must be clear that RAM 614 and its memory controller can be together considered as memory resources and each storage cell/row/array of RAM 614 can be considered as a random access memory device.

Per claims 63 and 65, Correale further teaches each of the requests for use of the push bus or pull bus sent from the memory resources comprises a target identifier identifying a target to receive data pushed from or pulled to the memory resources

(routing read data to a particular master requires the slave device providing target identification along with its claim/request of the read cycle and bus; see col. 4, lines 45-53, col. 5, lines 40-42).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-7, 16-21, 26-29, 33-35, 37, 40, 41, 43-45, 50, 51, 53, 54 and 57-60 are rejected under U.S.C. 103(a) as being unpatentable over Correale and Shaylor [US 6,408,325 B1] (hereinafter "Shaylor").

Per claims 1, 26 and 37, it is clear the Correale already teaches most of the claims as described above (the programming agent in claim 56 is considered to be equivalent to the processing agent of claim 1), and further teaches issuing a write command (the pulling of data from the processing agent to the memory resources must be a result of a write command) and loading data into an output transfer memory of the processing agent (see the rejection of claims 13, 49, 55, 56 and 61 above). Correale also discloses setting the output transfer memory to a read-only state, even though it does not explicitly recite this limitation. However, It should be clear that since

processors can execute instructions and issue memory write request much faster than the actual write operations can be completed by accessing the much slower memory, the processor's output register must have its write enable control signal disabled while the data to be written to memory is ready to be transferred over the data bus, in order to avoid the data being overwritten by a new write data generated by the processor before the current transfer is complete.

Correale does not teach executing a context. Shaylor teaches a multi-tasking and multi-threading processor that can enhance data processing efficiency (see Shaylor, col. 1, lines 46-50), the processor requires executing a context for each thread (see Shaylor, col. 1, lines 56-67). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine the teachings of Shaylor and Correale, in order to enhance data processing efficiency. As a result of the combination, Correale and Shaylor in combination teach "executing a context".

Per claims 2, 16 and 27, the combined teaching of Correale and Shaylor further discloses establishing a plurality of contexts (see Shaylor, col. 1, lines 56-67) on the processing agent and maintaining program counters (although not specified in Shaylor, it is clear that in a multi-tasking and multi-threading processor taught by Shaylor, there must be multiple program counters for the concurrently executing processes and threads) and context relative registers (see Shaylor col. 1, lines 20-32 and lines 56-67, col. 2, lines 1-27, col. 4, lines 37-67).

Per claims 3, 18, 28 and 50, the combined teaching of Correale and Shaylor further discloses the processing agent executes a context (see Shaylor, "context", col. 1, lines 56-67) and issues a read command to a memory controller in a read phase (see the rejection of claim 1 above, pushing data from the memory resources to the processing agent must be the result of a read command in a read phase).

Per claims 4 and 19, the combined teaching of Correale and Shaylor further discloses the memory controller processes the read command to be sent to one of the memory resources (see Correale, col. 5, lines 55-60, memory controller 704).

Per claims 5, 20, 29 and 51, the combined teaching of Correale and Shaylor further discloses the context is swapped out if the read data is required to continue the execution of the context (it is clear from the teaching of Shaylor that a context stores the state of a thread in memory and when a context switch occurs the context is saved to persistent storage, see Shaylor, col. 1, lines 56-67 and col. 2, lines 1-2; it is then further clear that if a read command issued by the thread requires data that is not stored in the memory that holds the context, then the context must be temporarily swapped out and stored in the persistent storage so that the context will not be overwritten by the acquired read data).

Per claim 6, the combined teaching of Correale and Shaylor further discloses after the memory controller has completed the processing of the read command, the memory controller pushes the data to an input transfer memory of the processing agent (see the rejection of claim 1 above for "input register").

Per claims 7 and 21, the combined teaching of Correale and Shaylor further discloses after the data has been pushed, the processing agent reads the data in the input transfer register (clearly the read data in the input register will be read by the processor) and the processing agent continues the execution of the context (see Shaylor, col. 1, lines 56-67, a context that was switched out must be switched back in to allow continued execution of the thread whose context was the switched out context).

Per claim 17, the combined teaching of Correale and Shaylor further discloses the context relative registers are selected from a group comprising of general purpose registers, inter-programming agent registers, static random access memory (SRAM) input transfer registers, dynamic random access memory (DRAM) input transfer registers, SRAM output transfer registers, DRAM output transfer registers, and local memory registers (see Shaylor, col. 1, lines 20-32 and lines 56-67, col. 2, lines 1-27, col. 4, lines 37-67).

Per claims 33, 40 and 54, the combined teaching of Correale and Shaylor further teaches the context is swapped out if the write command is required to continue the

execution of the context (it is clear from the teaching of Shaylor that a context stores the state of a thread in memory and when a context switch occurs the context is saved to persistent storage, see Shaylor, col. 1, lines 56-67 and col. 2, lines 1-2; it is then further clear that if a write command issued by the thread writes to the memory storing the context, then the context must be temporarily swapped out and stored in the persistent storage so that the context will not be overwritten by the write command).

Per claims 34 and 41, the combined teaching of Correale and Shaylor further discloses the memory controller pulls the data from the output transfer memory and the memory controller sends a signal to the processing agent to unlock the output transfer memory (following the discussion in the rejection of claim 1 above, if the output register is write disabled, then it must be re-enabled in order for future write data to be stored by the processor).

Per claim 35, the combined teaching of Correale and Shaylor further discloses if the context has been swapped out after the output transferred memory has been unlocked, the context is swapped back in and the processing agent continues the execution of the thread (Shaylor teaches a swapped out context must be switched back in to continue the thread's execution, since claim 34 teaches the swapping out is the result of a write command's possibility of overwriting the context, then it is clear that the context should be switched back in since re-enabling the output register indicates the write command is already completed).

Per claim 43-45, Correale further teaches the memory resources comprise memory controller channels (see Correale, col. 5, lines 54-60, memory controller 704 and PCI bridge 705).

Per claim 53, it is clear the claim is disclosed by claims 1, 26, 37 and 49 set forth above.

Per claims 57, 59 and 60, it is clear the claims are already disclosed by claims 1, 13, 49, 55, 56 and 61 as set forth above.

Per claim 58, it is clear the claim is already disclosed by claims 1, 13, 49, 55, 56 and 61 as set forth above.

Response to Arguments

11. Applicant's arguments with respect to claims 1-7, 13, 16-21, 26-29, 33-35, 37, 40-41, 43-45, 49-51 and 53-65 that the cited prior arts do not teach the newly added claim limitations (claims 1, 13, 26, 37, 49, 55, 56 and 61) and the newly added claims (claims 62-65) have been considered but are moot in view of the new ground(s) of rejection. The newly amended claim limitations and newly added claims are taught by Correale and Shaylor as set forth above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

/SHAWN GU/
25 March 2008

/Reginald G. Bragdon/
Supervisory Patent Examiner, Art Unit 2189